What is claimed is:

1. A method of manufacturing a semiconductor device, comprising:

providing a silicon-on-insulator (SOI) substrate which includes a silicon substrate having an upper surface, a first insulating layer having a lower surface extending horizontally over the upper surface of the silicon substrate, and a silicon layer having a lower surface extending horizontally over an upper surface of the first insulating layer;

forming a second insulating layer over an upper surface of the silicon layer of the SOI substrate;

implanting impurity ions into the silicon layer of the SOI substrate such that a peak ion concentration along a vertical depth of the silicon layer is located between an intermediate horizontal plane of the silicon layer and the lower surface of the silicon layer inclusive, wherein the intermediate horizontal plane extends horizontally within the silicon layer at half a vertical depth of the silicon layer; and

forming a gate electrode on the second insulating layer.

2. The method according to claim 1, wherein the impurity ions are a second conductivity type which is opposite from a first conductivity type, and wherein the semiconductor device is the first conductivity type.

3. A method of manufacturing a semiconductor device, comprising:

providing a silicon-on insulator (SOI) substrate which includes a silicon

substrat having an upper surface, a first insulating lay r having a lower surface extending horizontally over the upper surface of the silicon substrate, and a silicon layer having a lower surface extending horizontally over an upper surface of the first insulating layer;

forming a second insulating layer over an upper surface of the silicon layer of the SOI substrate;

forming a gate electrode over the second insulating layer; and

implanting impurity ions into the silicon layer of the SOI substrate at an oblique angle relative the upper surface of the silicon layer; wherein the impurity ions are implanted such that a peak ion concentration along a vertical depth of the silicon layer is located between an intermediate horizontal plane of the silicon layer and the lower surface of the silicon layer inclusive, and wherein the intermediate horizontal plane extends horizontally within the silicon layer at half a vertical depth of the silicon layer.

4. The method according to claim 3, wherein the impurity ions are a second conductivity type which is opposite from a first conductivity type, and wherein the semiconductor device is the first conductivity type.

5. A method of manufacturing a semiconductor device, comprising:

providing a silicon-on-insulator (SOI) substrate which includes a silicon substrate having an upper surface, a first insulating layer having a lower surface extending horizontally over the upper surface of the silicon substrate, and a silicon

layer having a lower surface xtending horizontally ov r an upper surface of the first insulating layer;

forming a second insulating layer over an upper surface of the silicon layer of the SOI substrate;

implanting impurity ions into the silicon layer of the SOI substrate such that a peak ion concentration along a vertical depth of the silicon layer is located between an intermediate horizontal plane of the silicon layer and the upper surface of the silicon layer, wherein the intermediate horizontal plane extends horizontally within the silicon layer at half a vertical depth of the silicon layer;

heat treating the silicon layer to diffuse the impurity ions implanted into the silicon layer such that an ion concentration of the silicon layer becomes substantially homogeneous along the vertical depth of the silicon layer.

6. The method according to claim 5, wherein the impurity ion is a second conductivity type which is opposite from a first conductivity type, and wherein the semiconductor device is the first conductivity type.

7. The method according to claim 5, wherein a temperature of the heat treatment is within a range of 950 ℃ ~ 1000℃

8. A method of manufacturing a semiconductor device, comprising:

providing a silicon-on-insulator (SOI) substrate which includes a silicon

substrate having an upper surfac , a first insulating layer having a lower surface extending horizontally over the upper surface of the silicon substrate, and a silicon layer having a lower surface extending horizontally over an upper surface of the first insulating layer;

forming a second insulating layer over an upper surface of the silicon layer of the SOI substrate;

implanting impurity ions into the silicon layer of the SOI substrate such that a peak ion concentration along a vertical depth of the silicon layer is located at the vertical depth 1/2 Tsoi $\pm$ 0.1 Tsoi of the silicon layer, where Tsoi is an entire vertical depth of the silicon layer; and

forming a gate electrode over the second insulating layer.

9. The method according to claim 8, wherein the impurity ions are a second conductivity type which is opposite from a first conductivity type, and wherein the semiconductor device is the first conductivity type.